ABSTRACT

So as to generate multiple output signals whose phases are evenly spaced about 360 degrees, and having a frequency equal to that of an input signal, a phase multiplier circuit includes three or more instances of a phase multiplier subcircuit and additional circuitry configured in a negative feedback loop. Each phase multiplier subcircuit includes a difference circuit, a loop filter transistor, and a voltage-controlled delay circuit. The difference circuit converts to a phase current a delay from an input signal to the delay circuit to an output signal from the delay circuit, and subtracts from the phase current a bias current proportional to the smallest positive delay from the output signal with the largest phase to the output signal with the smallest phase. The subtracted current is integrated by the loop filter transistor, and steady-state operation is achieved when for each phase multiplier subcircuit, the bias current is equal to the phase current. Evenly spaced phases of the output signals about 360 degrees are achieved when the delay to phase current gain and delay to bias current gain are substantially equal.